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10/075,938	02/13/2002	Yue Der Chih	67,200-489	9831

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TUNG & ASSOCIATES
Suite 120
838 W. Long Lake Road
Bloomfield Hills, MI 48302

EXAMINER	
BAKER, STEPHEN M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,938	CHIH, YUE DER	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

In [007]: in line 7, "ungradable" apparently should be "upgradeable".

In [008]: in line 11, "either or" apparently should be deleted, as row and column selection are both apparently necessary in order to access a single "memory cell".

In [009]: in line 3, "or" apparently should be "and"; in line 10, "elements" apparently should be "element".

In [0010]: in line 4, "or data" is needlessly redundant and thus distractive and apparently should be deleted; in line 11, "read-out" apparently should be 'obtained", as data that is "read out" is data as it exists prior to correction by ECC processing.

in lines 13-14, "the defective rows or columns itself are" is grammatically incorrect, apparently misdescriptive, and apparently should be "a defective column itself is", as defective bit lines in the information array are the relevant context and as correction of all data in a defective row of the information array is apparently not within the capacity of the ECC scheme, which apparently can only correct a bitline-caused error, which affects a single bit of a word, but cannot correct a wordline-caused error, which affects all the bits of a word.

In [0011]: in line 4, "columns" apparently should be "rows and columns".

In [0017]: in line 6, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array" as a "latch" is customarily used to refer to logic capable of storing

only a single bit; in line 9, "to thereby identify and repair defective row or columns" apparently should be "for identifying and repairing defective rows or columns"; in lines 10-11, "regardless of the corruption of the columns" apparently should be "despite an error caused by a defective column" as the disclosed ECC corrects a single bit error and as the columns correspond to bits of the repairing word read out, reading out the repairing word array ("information array") being relevant to the context; in line 19, 'read-out" apparently should be "obtained".

In [0018]: in lines 4, 5, 13 and 14-15 "volatile latch" apparently should be "volatile latches" or "volatile latch array"; in lines 5-7, "The decoder circuit is generally linked to the ECC circuit, while the decoder circuit is generally linked to the information array" apparently should be "The decoder circuit is generally linked to the volatile latch array and to the information array" or "The decoder circuit is generally linked to the volatile latches and to the information array"; in line 9, "includes" apparently should be "include".

In [0024]: in line 2, "column" apparently should be "row and column".

In [0025]: in line 1, "column" apparently should be "row and column".

In [0031]: in lines 6-7, "relied upon as a" apparently should be "used as the".

In [0032]: in line 2, "be another type of non-volatile memory device that can" apparently should be deleted.

In [0034]: in line 2, "column" apparently should be "row and column"; in lines 3 and 7, "information or data" apparently should be "information"; in line 4, "correction or repair" apparently should be "repair" as "correction" is customarily a data (software) concept, and "repairing" is customarily a hardware concept.

In [0035]: in line 8 and lines 9-10, "defective or corrupted" apparently should be "defective", as "corruption" is customarily a software (data) concept; in lines 8-9, "defective or corruptive" apparently should be "defective".

In [0038]: in lines 2 and 9, "column" apparently should be "row and column"; in line 13, "detection" apparently should be "detection and correction".

In [0039]: in line 6, "column" apparently should be "row and column"; in lines 6-7, "information or data" apparently should be "information"; in lines 9 and 13, "repair" apparently should be "correct"; in lines 10-11, "corrupt or defective" apparently should be "defective"; in line 14, "read out of" apparently should be "obtained from"; in line 15, "defective or corrupted" apparently should be "defective".

In [0040]: in line 4, "read" apparently should be "obtained"; in lines 4-5, "defective or corrupted bits are present" apparently should be "a corrupted bit is present", as the disclosed Hamming code is apparently only a single-error correcting code; in line 8, "defective" apparently should be "corrupted".

In [0041]: in line 7, "a volatile latch" apparently should be "volatile latches"; in line 10, "to thereby identify and repair" apparently should be "for identifying and repairing" as the information must first be stored in the volatile latch array before being used to identify and repair (locate and replace by substitution) defective rows and/or columns; in line 12, "regardless of the corruption of the columns" apparently should be "despite an error in the repairing information caused by a defective column"; in line 15, "correct correctable errors" apparently should be "correct a correctable error" as the disclosed Hamming code is apparently a single-error correcting code; in lines 17-18, "Y-address

corresponding to a defective column or row" apparently should be "Y-address corresponding to a defective column", as a "Y-address" is conventionally used to designate a column address, although "row" and "column" are otherwise evidently interchangeable by simple physical rotation.

In [0043]: in lines 1-3, "The number of spare columns depends on the coding of ECC circuit 70 and the maximum number of defective columns on a normal array that can be repaired" apparently should read as "The number of spare columns determines the maximum number of defective columns on a normal array that can be repaired", as there is no understandable disclosed relationship between the ECC correction capacity, which is a data recovery technique, and the "repair" capacity, which is a hardware replacement technique; regarding line 5, it is noted that "Hamming code (5, 16)" is unconventional notation that lacks explanation, and apparently should be "a (16, 11) Hamming code", which is a SEC-DED code, meaning it can correct only single errors in codewords; in lines 3-10, "For example, in a scenario in which 512 columns are designated in a normal array, and a data bus comprises 16-bits, assuming that Hamming code (5, 16) is utilized and additionally assuming that the maximum number of defective columns that can be repaired is 4, then the number of spare columns required can be calculated as 20 based on the value 4x5. This holds true because 5 spare columns are generally required to repair 4 defective columns." appears to be largely a non-sequitur, as the relevance of the total number of columns (512) to the number of spare or repairable columns is not apparent, the required Hamming code length is apparently already determined by the data bus width (16) and thus of no

further apparent relevance, the multiplier of "4" in "4x5" is not adequately explained, and the requirement of 5 spare lines to repair 4 defective lines is not adequately explained, and apparently should be "In one embodiment, there are 512 columns in the array, the data bus is 16 bits, and a (16, 11) Hamming code is used. A total of 20 spare columns are provided, each spare being assignable to one of four sets of four I/O terminals and five spares being reserved for each such set of four I/O terminals".

In [0044]: the entire paragraph is largely a non-sequitur that serves no apparent useful purpose and apparently should be deleted or amended to read as "Traditionally, each spare column is reserved for repairing one column corresponding to a specific I/O terminal. If there are 16 I/O terminals for a 16-bit data bus, then 16 spare columns would normally be required to support a one-time repair of any possible column out of the 16 columns accessed at one time. To improve repairing efficiency, the columns for two or more I/O terminals can be made to share a single spare column, in a more complicated design. In the specific embodiment described above, all columns associated with a set of four I/O terminals share a single set of five spare columns. The (16, 11) Hamming code is well known in the art and is described at page 64 or "Error Control Coding: Fundamentals and Applications" by Shu Lin & Daniel J. Costello, Jr."

Appropriate correction is required.

2. The abstract of the disclosure is objected to because "to thereby identify and repair defective columns or rows associated with the non-volatile memory, regardless of the corruption of the columns" apparently should be "for identifying and repairing

defective columns or rows associated with the non-volatile memory, despite errors in the repairing data read out".

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1: in line 4, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array", as a single latch by itself is apparently incapable of storing data sufficient for "repairing"; in lines 6-9, "enabling an error correction coding circuit during reading of said repairing data to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows" appears to be misdescriptive, prolix in some parts and elliptical in other parts, and apparently should be "enabling an error correction coding circuit during reading of said repairing data, for identifying and repairing defective columns or rows associated with said non-volatile memory despite corruption of the repairing data as read".

In claim 2: in line 4, "to thereby correct correctable errors if a particular address" apparently should be "for correcting a correctable error if a particular address"; in lines 5-6, "column or row" apparently should be "column".

In claim 3: in line 3, "column or row" apparently should be "column".

In claim 4: the specification's description of connections shown in Fig. 6 has apparently been paraphrased to generate an otherwise non-existent method of "linking" and "connecting" the elements shown. It is here noted that there is apparently no distinction between a "link" and a "connection" as these terms are arbitrarily used by applicant, and the term "linking" is apparently used where no direct connection exists *i.e.* between the "error correction coding circuit" 70 and the row-column "decoder" 62. In lines 2-4, "linking a read circuit to said main array to thereby permit data to be read from said main array and transmitted to said error correction coding circuit" apparently should be "using a read circuit linked to said main array to read data from said main array and to transmit the read data to said error correction coding circuit"; in lines 5-7, "connecting said error control circuit to said volatile latch to thereby permit data to be transferred" apparently should be "said error control circuit being connected to said volatile latches to permit data to be transferred" or "said error control circuit being connected to said volatile latch array to permit data to be transferred"; in lines 7-11, "and linking a decoder circuit to said error correction coding circuit, such that said decoder circuit is linked to said information array, at least one spare row, and said main array, wherein" apparently should be "said error correction coding circuit being linked to a decoder circuit, and thereby to said information array, at least one spare row and said main array, and wherein".

In claim 5: "linking said volatile latch to said decoder circuit to thereby permit data" apparently should be "using a link between said volatile latches and said decoder

circuit to permit data" or "using a link between said volatile latch array and said decoder circuit to permit data".

In claim 6: in line 3, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array"; in line 4, the comma apparently should be deleted; in line 8, "column-repairing" apparently should be "repairing", to agree with line 2; in line 9, "non-volatile memory" apparently should be "volatile latches" or "volatile latch array".

In claim 7: in line 4, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array"; in line 8, "to thereby correct correctable errors if a particular address" apparently should be "for correcting a correctable error if a particular address", as "enabling" an error correction circuit does not, by itself, correct any data, and as the disclosed (16, 11) Hamming SEC-DED ECC apparently can correct only a single error at each address (16-bit word per address); in line 11, "corresponding to said at least one defective column or row" apparently should be deleted.

In claim 8: in line 4, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array"; in line 5, "said column repair data" is inconsistent with line 3 and apparently should be "said repairing data"; in lines 7-9, "an error correction coding circuit linked to said volatile latch and a decoder circuit" apparently should be "an error correction coding circuit linked to said volatile latches and thereby to a decoder circuit" or "an error correction coding circuit linked to said volatile latch array and thereby to a decoder circuit"; in lines 11-12 "to thereby correct correctable errors if a particular address" apparently should be "for correcting a correctable error if a particular address";

in lines 14-15, "corresponding to said at least one defective column or row" apparently should be deleted.

In claim 9: in line 4, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array"; in line 5, "said column repair data" apparently should be "said repairing data"; in line 8, "said volatile latch" apparently should be "said volatile latches" or "said volatile latch array", and "a decoder" apparently should be "thereby to a decoder"; in lines 10-13, "enabling an error correction coding circuit during reading of said repairing data to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows" apparently should be "enabling an error correction coding circuit during reading of said repairing data, for identifying and repairing defective columns or rows associated with said non-volatile memory despite corruption of the repairing data as read".

In claim 10: in line 4, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array"; in line 7, "said column repair data" apparently should be "said repairing data"; in lines 9-10, "said volatile latch" apparently should be "said volatile latches" or "said volatile latch array"; in line 10, "a decoder" apparently should be "thereby to a decoder"; in lines 11-14, "enabling an error correction coding circuit during reading of said repairing data to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows" apparently should be "enabling an error correction coding circuit during reading of said repairing data, for identifying and repairing defective columns or rows associated with said non-volatile memory despite corruption of the repairing data as read".

In claim 11: in line 3, "reading circuit" apparently should be "a reading circuit"; in lines 4-5, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array"; in lines 6-9, "enabling an error correction coding circuit during reading of said repairing data to thereby identify and repair defective columns or rows associated with said non-volatile memory regardless of the corruption of said columns or rows" apparently should be "enabling an error correction coding circuit during reading of said repairing data, for identifying and repairing defective columns or rows associated with said non-volatile memory despite corruption of the repairing data as read".

In claim 12: in line 4, "to thereby correct correctable errors if a particular address" apparently should be "for correcting a correctable error if a particular address"; in lines 5-6, "column or row" apparently should be "column".

In claim 13: in line 3, "column or row" apparently should be "column".

In claim 14: in line 1, "further comprising" apparently should be "further wherein"; in line 2, "linked" apparently should be "is linked"; in line 3, "and transmitted" apparently should be "to be transmitted"; in line 5, "connected' apparently should be "is connected"; in lines 5 and 7, "said volatile latch" apparently should be "said volatile latches" or "said volatile latch array"; in lines 8-12, "a decoder circuit linked to said error correction coding circuit, such that said decoder circuit is linked to said information array, at least one spare row, and said main array, wherein" apparently should be "said error correction coding circuit is linked to a decoder circuit, and thereby to said information array, at least one spare row and said main array, and wherein".

In claim 15: in line 1, "further comprising" apparently should be "further wherein"; in line 2, "linked" apparently should be "is linked".

In claim 16: in line 5, "non-volatile memory" apparently should be "volatile latches" or "volatile latch array".

In claim 17: in line 3, "read circuit" apparently should be "a read circuit"; in lines 4-5, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array"; in lines 7-8, "to thereby correct correctable errors if a particular address" apparently should be "for correcting a correctable error if a particular address"; in line 11, "corresponding to said at least one defective column or row" apparently should be deleted.

In claim 18: in line 3, "read circuit" apparently should be "a read circuit"; in lines 4-5, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array"; in lines 5-6, "wherein said column repair data is read utilizing a read circuit linked" is redundant with lines 3-4, except where it incorrectly disagrees with "repairing data" in line 3, and apparently should be "wherein said read circuit is linked"; in lines 8-9, "linked to said volatile latch and a decoder circuit" apparently should be "linked to said volatile latches and thereby to a decoder circuit" or "linked to said volatile latch array and thereby to a decoder circuit"; in lines 9-10, "and said error correction coding circuit enabled" apparently should be "wherein said error correction coding circuit is enabled"; in lines 11-12, "to thereby correct correctable errors if a particular address" apparently should be "for correcting a correctable error if a particular address"; in lines 14-15, "corresponding to said at least one defective column or row" apparently should be deleted.

In claim 19: in lines 4-5, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array"; in lines 5-6, "wherein said column repair data is read utilizing a read circuit linked" apparently should be "wherein said read circuit is linked"; in lines 8-9, "linked to said volatile latch and a decoder circuit" apparently should be "linked to said volatile latches and thereby to a decoder circuit" or "linked to said volatile latch array and thereby to a decoder circuit"; in line 10, "enabled" apparently should be "is enabled"; in line 11, "to thereby identify and repair" apparently should be "for identifying and repairing"; in line 13, "regardless of corruption of said columns or rows" apparently should be "despite corruption of the repairing data as read".

In claim 20: in lines 4-5, "a volatile latch" apparently should be "volatile latches" or "a volatile latch array"; in lines 7-8, "wherein said column repair data is read utilizing a read circuit linked" apparently should be "wherein said read circuit is linked"; in line 10, "linked to said volatile latch and a decoder circuit" apparently should be "linked to said volatile latches and thereby to a decoder circuit" or "linked to said volatile latch array and thereby to a decoder circuit"; in line 11, "enabled" apparently should be "is enabled"; in line 12, "to thereby identify and repair" apparently should be "for identifying and repairing"; in line 14, "regardless of corruption of said columns or rows" apparently should be "despite corruption of the repairing data as read".

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,471,478 to Mangan *et al* (hereafter Mangan).

Mangan discloses an EEPROM "non-volatile" memory system of the 'flash' variety, for storing sector-sized (512-byte) data blocks. Referring to Fig. 3, a typical block (205) in Mangan's system includes a data sector portion (207) and an overhead portion (209), both of which extend across all four rows of a block and share common column addresses (col. 5, lines 14-20). Data is preferably read one row at a time (col. 5, lines 28-29). Data transfers between the EEPROM modules and an associated storage controller occur in eight-byte 'chunks'. Fig. 4 shows the data sector in terms of the chunks, there being 18 chunks in each of the four rows of a block.

Mangan's overhead portion includes "repairing data" indicating the address of a replacement block, if the associated data block is defective. The overhead data is protected by ECC, as is the data block itself. Mangan's storage controller (133) requires an "error correction coding circuit", necessarily "enabled", within. Mangan's block data defects are presumably the result of defective rows or columns in the EEPROM modules (131, 132), and so Mangan's interpreting of the overhead data is presumably to "identify and repair (i.e. appropriately substitute alternative storage cells for) defective columns or rows associated with said non-volatile memory".

Mangan's storage controller necessarily stores ECC-corrected overhead data internally, however the internal circuitry of Mangan's controller is not shown. Thus

Mangan does not show a "volatile latch" in the storage controller (133) for the internal storing required by Mangan's storage controller during interpreting of the defect information included in the overhead. Official Notice is given that using a "volatile latch" as a processor register was conventional practice at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the internal registers of Mangan's storage controller by "volatile latches". Such an implementation would have been obvious because using a "volatile latch" as a processor register was already mere conventional practice.

Further regarding claims 3, 7, 8 and 13, the architecture of Mangan's EEPROM modules is not shown. Thus, Mangan does not show X-Y addressing in the EEPROMs. Official Notice is given that using X-Y addressing in EEPROMs was conventional practice at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the EEPROM addressing architecture of Mangan's system by means of X-Y addressing. Such an implementation would have been obvious because X-Y addressing in EEPROMs was already mere conventional practice.

Further regarding claims 4, 14, the architecture of Mangan's EEPROM modules is not shown. Thus, Mangan does not show spare rows and columns in the EEPROMs. Official Notice is given that including spare rows and columns in EEPROMs was conventional practice at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the EEPROMs with EEPROMs having spare rows and columns. Such an

implementation would have been obvious because including spare rows and columns in EEPROMs was already mere conventional practice.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (703) 305-9681. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb